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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,484	07/29/2003	Christian A.J. Lutkemeyer	13433US05	7455

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EXAMINER	
LAM, TUAN THIEU	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,484	LUTKEMEYER, CHRISTIAN A.J.	
	Examiner	Art Unit	
	Tuan T. Lam	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-21 and 30-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-21 and 30-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the preliminary amendment filed 7/29/2003. Claims 18-21 and 30-40 are pending.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 18, 30-32 and 39-40 are rejected under 35 U.S.C. 102(b) as being anticipated by Hillis et al. (USP 5,118,975). Figure 2 of Hillis et al. shows a circuit comprising a rising edge phase comparator (32A) for comparing a phase of a first signal (SYS CLK IN) associated with a first signal level (high/low) with a phase of a second signal (DEL CLK OUT REF) associated with a second signal level (low/high), and for generating a rising edge compensation signal (output of the rising edge phase comparator), a falling edge phase comparator (32B) for comparing a phase of a first signal (SYS CLK IN) associated with a first signal level (high/low) with a phase of a second signal (DEL CLK OUT REF) associated with a second signal level (low/high), and for generating a falling edge compensation signal (output of the falling edge phase comparator), an adjustable delay buffer (20 shown in figure 1 and details shown in figures 3a-3b) as called for in claims 18 and 32.

Regarding claims 30 and 39, a power supply (not shown) for providing a plurality of supply voltages VCC/VDD and ground associated with the high and low logic levels of the first and second signals.

Regarding claims 31 and 40, the first and second clock signals are derived from the source (not shown) that generates the SYS CLK IN of figure 1.

Claims 18, 30-33 and 39-40 are rejected under 35 U.S.C. 102(b) as being anticipated by Masleid (USP 5,828,257). Figure 2 shows phase locked circuit comprising a rising edge phase comparator (34) of a first signal (output of buffer 10 associated with a first signal level (high/low) with a rising edge of a second signal (20) associated with a second signal level (low/high), and for generating a rising edge compensation signal (41) a falling edge phase comparing (36) for comparing a falling edge of the first signal associated with a first signal level (high/low) with a falling edge of the second signal associated with a second signal level (low/high), and for generating a falling edge compensation signal (43), an adjustable delay buffer (38, 40, 12, 14, 16, 18) coupled to the rising and falling edge comparators as called for in claims 18 and 32.

Regarding claims 30 and 39, a power supply (not shown) for providing a plurality of supply voltages VCC/VDD and ground associated with the high and low logic levels of the first and second signals.

Regarding claims 31 and 40, the first and second clock signals are derived from the source (not shown) that generates the clock input 20.

Regarding claim 33, figure 2 shows a buffer transistor 16.

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or

improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 18-21 and 32-38 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-3 of U.S. Patent No. 6,636,091. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are claiming common technical features.

Regarding claim 18, claim 1 of USP 6,636,091 recites a rising edge comparator, a falling edge comparator, a adjustable delay buffer.

Regarding claims 19 and 33-35, claim 1 of USP 6,636,091 further recites adjustable delay buffer comprising a buffer transistor, a rising edge control transistor, a falling edge control transistor.

Regarding claims 20 and 36-37, claim 2 of USP 6,636,091 recites rising edge comparator comprises a register and a falling edge comparator comprises a register.

Regarding claims 21 and 38, claim 3 of USP 6,636,091 recites low pass filters.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 703-305-3791. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Tuan T. Lam
Primary Examiner
Art Unit 2816

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March 22, 2005